

# **JEDEC STANDARD**

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## **Thermal Test Environment Modifications for MultiChip Packages**

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**JESD51-31**

**JULY 2008**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## **THERMAL TEST ENVIRONMENT MODIFICATIONS FOR MULTICHIP PACKAGES**

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### **Foreword**

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This document was prepared by the JEDEC JC15 committee to document appropriate modifications needed for Multi-Chip Packages using the thermal test environmental conditions specified in the JESD51 series of specifications.

Multi-Chip Packages as described in the overview document of this series of specifications are packages with more than one distinct heat source.

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### **Introduction**

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Multi-Chip Packages as described in the overview document of this series of specifications are packages with more than one distinct heat source. Because the thermal performance of the package can change with the proportion of heat dissipated in each source, more detailed information is required to specify the thermal performance of the packages than is required for a single chip package.

Multi-Chip Packages can be separated into two general types: (1) packages which are symmetrical in the x-y directions relative to the center, and (2) packages for which the chips or heat sources are distributed and there is no assumption of symmetry for the heat sources.



## THERMAL TEST ENVIRONMENT MODIFICATIONS FOR MULTICHIP PACKAGES

(From JEDEC Board Ballot JCB-08-34, formulated under the cognizance of the JC-15 Committee on electrical and Thermal Characterization Techniques for Electronic packages and Interconnects.)

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### 1 Scope

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This document specifies the appropriate modifications needed for Multi-Chip Packages to the thermal test environmental conditions specified in the JESD51 series of specifications. The data obtained from methods of this document are the raw data used to document the thermal performance of the package. The use of this data will be documented in JESD51-XX, “Guideline to Support Effective Use of MCP Thermal Measurements” which is being prepared.

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### 2 Normative references

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The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

1. JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)*. This is the overview document for this series of specifications.
2. JESD51-1, *Integrated Circuit Thermal Measurement Method - Electrical Test Method*.
3. JESD51-2, *Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*.
4. JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
5. JESD51-4, *Thermal Test Chip Guideline (Wire Bond Type Chip)*.
6. JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*.
7. JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*.

## 2 Normative references (cont'd)

8. JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

9. JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*.

10. JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.

11. JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*.

12. JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*.

13. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*.

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## 3 Terms and definitions

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For the purposes of this standard, the terms and definitions given in JESD51 series of specifications<sup>1-13</sup> and the following apply:

MCP: Multi-Chip Package. A package containing more than one heat source.

$\Delta T_{JiA}(P1, P2, \dots Pn)$  or  $\Delta T_{-JiA}(P1, P2, \dots Pn)$ : Temperature rise for each source,  $i$ , relative to the ambient temperature at the power dissipation of  $P1$ ,  $P2$ , etc for source 1, 2, etc.

$\Delta T_{TA}(x,y)(P1, P2, \dots Pn)$  or  $\Delta T_{-JT}(x,y) (P1, P2, \dots Pn)$ : Temperature rise of the top of the package relative to the ambient temperature at the power dissipation of  $P1$ ,  $P2$ , etc for source 1, 2, etc. Because the center of the package may not be the hottest spot on the package top, the location that the temperature was taken is given in  $x,y$  (horizontal, vertical) dimensions with the pin 1 or A1 location in the lower left corner. See Figure 1 for a sketch of the orientation.

$\Delta T_{BA}(S,E,N,W)(P1, P2, \dots Pn)$  or  $\Delta T_{-BA}(P1, P2, \dots Pn)$ : Board temperature rise relative to ambient for each board temperature on the South, East, North, and West sides of the package with the pin 1 or A1 location in the lower left corner. The board temperature is measured on the top surface of the board as specified in JESD51-8. See Figure 1 for a sketch of the orientation.

$\Delta T_{JiX}(P1, P2, \dots Pn)$  or  $\Delta T_{-JiX}(P1, P2, \dots Pn)$ : Temperature rise for each source,  $i$ , relative to a reference temperature at the power dissipation of  $P1$ ,  $P2$ , etc for source 1, 2, etc.



### 3 Terms and definitions (cont'd)

$\Delta T_{TX}(x,y)(P1,P2,\dots Pn)$  or  $\Delta T_{TX}(x,y)(P1,P2,\dots Pn)$ : Temperature rise of the top of the package relative to a reference temperature at the power dissipation of P1, P2, etc for source 1, 2, etc. Because the center of the package may not be the hottest spot on the package top, the location that the temperature was taken is given in x,y (horizontal, vertical) dimensions with the pin 1 or A1 location in the lower left corner. See Figure 1 for a sketch of the orientation.

$\Delta T_{BX}(S,E,N,W)(P1,P2,\dots Pn)$  or  $\Delta T_{BX}(P1,P2,\dots Pn)$ : Board temperature rise relative to a reference temperature for each board temperature on the South, East, North, and West sides of the package with the pin 1 or A1 location in the lower left corner. The board temperature is measured on the top surface of the board as specified in JESD51-8.

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## 4 Junction-to-Ambient thermal measurement

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This section applies to the junction-to-ambient thermal dissipation using the environment specified by JESD51-2 and JESD51-6 for natural convection (still air) and forced convection respectively.

### 4.1 Test boards

The test boards are specified in JESD51 series of specifications<sup>4,6,8,10-12</sup> with an additional document being prepared which describes the changes that may be required for some MCP packages because of the additional connections required to power up all the heat sources and measure the junction temperatures.

### 4.2 Power used for testing

#### 4.2.1 Test chips with individual power control

Because natural convection thermal performance depends on the surface temperature of the package, JESD51-2 recommends power levels based on a 30 °C to 60 °C temperature rise at the heat source. If the package can be assembled with thermal die and wired to permit individual control of each heat source, it is recommended to use the power levels recommended in JESD51-2. The ideal way to test the package is to power each heat source individually at the recommended power level and measure the temperature rise of all the sources. This technique provides the full matrix of temperature rises that can be used to calculate performance with any arbitrary power distribution using superposition techniques. The amount of power applied to each source must be in a reasonable range for the size and characteristics of the source.

If the power distribution for the heat sources is known, the temperature rise of each source can be measured with that power distribution. Knowing the use conditions of the device will help determine a reasonable set of measurements to cover the expected range of use.

## **4.2 Power used for testing (cont'd)**

### **4.2.2 Testing without individual power control.**

Because it may be impossible to control the power at each heat source, the alternative approach is to measure the performance of the package using the available range of power for each heat source with a temperature rise large enough that the resolution of the temperature measurement of the heated sources using the temperature sensitive parameter is at least 1% of the temperature rise or 0.2 °C, whichever is the larger value.

## **4.3 Test results**

### **4.3.1 Steady state determination**

Steady state is defined when all of the measurement points are changing slow enough that waiting an additional time will not improve the accuracy of the measurement. The recommended method is documented in Section 3.6 of JESD51-1 with the measured temperature rise substituted for the thermal resistance. It should be noted that this procedure will cause an early termination of the measurement unless the algorithm is started after the system is close to a steady state condition or “appears to have reached steady state.” It also should be noted that all the measurement points must reach steady state, not just the powered heat sources.

### **4.3.2 Junction or source temperature rise**

The junction temperature rise,  $\Delta T_{JiA}(P1, P2, \dots Pn)$  for each heat source,  $i$ , at each power distribution tested is reported relative to the ambient temperature.

### **4.3.3 Board temperature**

The board temperature rise,  $\Delta T_{BA}(S, E, N, W)(P1, P2, \dots Pn)$ , may be reported at each side of the package for each of the power conditions tested. Figure 1 shows the location of the S, E, N, or W side of the package. For an MCP that has both x and y symmetry relative to the package center, only one board temperature rise is needed. The board temperature is measured as described in JESD51-8 [9].

### **4.3.4 Top of package temperature**

A thermocouple reading on the top of the package is extremely useful for determining the junction temperatures in an application as described in JESD51-12 [13]. For simplicity in reporting the measurements, the temperature rise at the top of the package relative to ambient is reported,  $\Delta T_{TA}(x, y)(P1, P2, \dots Pn)$ . The location of the top of package thermocouple should be chosen to give the most accurate means of estimating the maximum junction temperature of the MCP. Typically, the hottest accessible location on the surface is chosen.

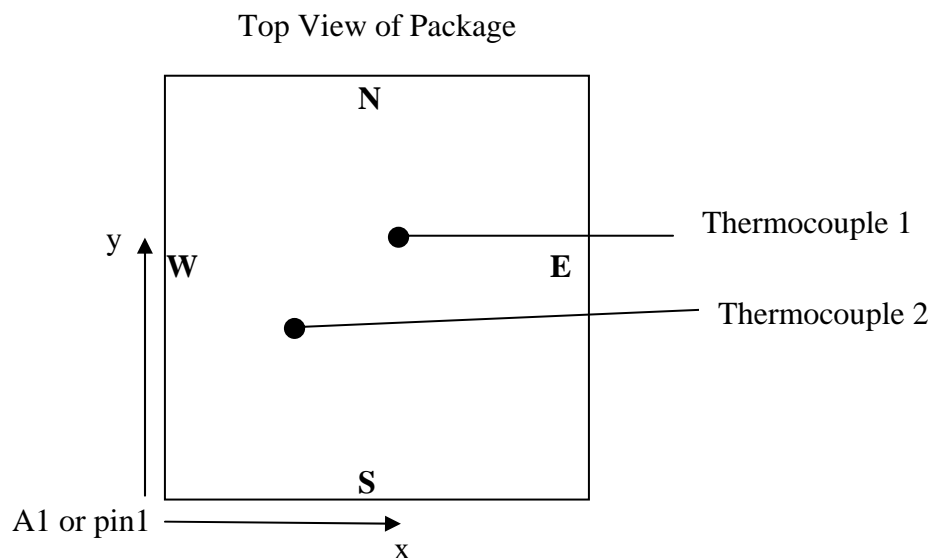
### 4.3 Test results (cont'd)

#### 4.3.4 Top of package temperature (cont'd)

The locations of the top of package measurement must be given as the x,y (horizontal, vertical) distance from the A1 corner of the package when the A1 corner is located in the lower left corner and the package is viewed from the top of the package as shown in Figure 1.

The accuracy by which the junction temperatures of the heat sources can be derived from the top of package thermocouple reading will depend on the structure inside the package and the range of power values for which data is provided. As an example, when there is a cooler die above the hotter die and the cooler die is closer to the surface where the package thermocouple is placed, the thermocouple will reflect the temperature of the closer heat source better than the hotter source below. The issue can be minimized by the choice of power combinations used when reporting the data.

More than one package thermocouple may be used provided that the number of thermocouples does not lower the temperature rise of the heat sources more than 2%. Thermistors can be used in place of thermocouples. Measurements using an IR camera will yield more data, especially for packages with many heat sources.



**Figure 1 — Illustration of the x,y location of two thermocouples and the N, E, S, or W side of the package.**

#### 4.4 Test method summary

The test method using the same procedures and methods specified in JESD51-2 and JESD51-6 except that heat sources must be powered and the results obtained for a matrix of powers for the various sources that will either match the power distributions of the MCP in the application or provide the data to allow calculation of the appropriate power distribution using superposition techniques. The use of superposition techniques will be documented in JESDXX, “Guideline to Support Effective Use of MCP Thermal Measurements” which is being prepared.

#### 4.5 Example results table

There are many different ways to arrange and report the data. For this example, we assume four chips in an array package with the four chips attached to the substrate in a MCP, with the ability to separately control the power to each chip. In this case, the measurements were taken with five different power configurations.

**Table 1 — Example of Data reporting table**

<b>Type of Thermal Resistance Measurement</b>							
<b>Reference Temperature Location and Description</b>							
			<b>Test1</b>	<b>Test 2</b>	<b>Test 3</b>	<b>Test 4</b>	<b>Etc</b>
<b>Power P1</b>							
<b>Power P2</b>							
<b>Power P3</b>							
<b>Power P4</b>							
$\Delta T_{J1X}$							
$\Delta T_{J2X}$							
$\Delta T_{J3X}$							
$\Delta T_{J4X}$							
$\Delta T_{TX1}(X,Y)$	X loc	Y loc					
$\Delta T_{TX2}(X,Y)$	X loc	Y loc					
$\Delta T_{BX}(S)$							
$\Delta T_{BX}(E)$							
$\Delta T_{BX}(N)$							
$\Delta T_{BX}(W)$							

It is extremely important that the reference temperature location be given for the measurement and that the same measurement location used for all the data collected for this table. This data is only an example assuming that data at two top package temperature locations would be reported along with the X,Y location for each measurement point.

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**5 Junction-to-Board Reference Environment for MCP packages**

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This section applies to the junction-to-board heat dissipation using the environment specified by JESD51-8 with modifications to better accommodate asymmetric heat flow which is more likely to be found in MCPs.

**5.1 Test boards**

The test boards must have two internal conducting planes. The test boards are specified in JESD51 series of specifications [6,8,10,11,12] with an additional document being prepared which describes the changes that may be required for some MCP packages because of the additional connections required to power up all the heat sources and measure the junction temperatures.

**5.2 Power used for testing****5.2.1 Test chips with individual power control**

If the package can be assembled with thermal die and wired to permit individual control of each heat source, it is recommended to use the power to achieve a 15 °C to 30 °C temperature rise recommended in JESD51-8. The ideal way to test the package is to power each heat source individually at the recommended power level and measure the temperature rise of all the sources. This technique provides the full matrix of temperature rises that can be used to calculate performance with any arbitrary power distribution using superposition techniques. The amount of power applied to each source must be in a reasonable range for the size and characteristics of the source.

If the power distribution for the heat sources is known, the temperature rise of each source can be measured with that power distribution. Knowing the use conditions of the device will help determine a reasonable set of measurements to cover the expected range of use.

**5.2.2 Testing without individual power control**

Because it may be impossible to control the power at each heat source, the alternative approach is to measure the performance of the package using the available range of power for each heat source with a temperature rise large enough that the resolution of the temperature measurement of the source using the temperature sensitive parameter is at least 1% of the temperature rise or 0.2 °C, whichever is the larger value.

## 5.3 Test results

### 5.3.1 Steady state determination

Steady state is defined when all of the measurement points are changing slow enough that waiting an additional time will not improve the accuracy of the measurement. The recommended method is documented in Section 3.6 of JESD51-1 with the measured temperature rise substituted for the thermal resistance. It should be noted that this procedure will cause an early termination of the measurement unless the algorithm is started after the system is close to a steady state condition or “appears to have reached steady state.” It also should be noted that all the measurement points must reach steady state, not just the powered heat sources.

### 5.3.2 Junction or source temperature rise

The junction temperature rise,  $\Delta T_{JiX}(P1, P2, \dots Pn)$  for each heat source,  $i$ , at each power distribution tested is reported relative to a reference temperature. JESD51-8 specifies that the water cooled ring cold plate ring be maintained close to room temperature. The recommended reference temperature for this measurement is the temperature of the board when the package and board are in equilibrium with the ring cold plate prior to the beginning of the test. An alternate technique uses the temperature of the ring cold plate at a specified location.

### 5.3.3 Board temperature

Board temperature rise,  $\Delta T_{BX}(S, E, N, W)(P1, P2, \dots Pn)$ , relative to the reference temperature is measured for each board temperature on the South, East, North, and West sides of the package with the pin 1 or A1 location in the lower left corner at the sides of the package as shown in Figure 1. The board temperature is measured on the top surface of the board as specified in JESD51-8. MCP packages which are not completely symmetric should have the board temperature measured at all four sides of the package. The same reference temperature used in Section 5.3.2 must be used.

### 5.3.4 Top of package temperature

A top of package temperature is not needed in the junction-to-board environment, but is frequently included to provide more information for simulation validation. The temperature rise at the top of the package relative to the reference temperature is reported,  $\Delta T_{TX}(x, y)(P1, P2, \dots Pn)$ . The location of the top of package thermocouple should be chosen to give the most accurate means of estimating the maximum junction temperature of the MCP. Typically, the hottest accessible location on the surface is chosen. The location of the top of package measurement must be given as the  $x, y$  (horizontal, vertical) distance from the A1 corner of the package when the A1 corner is located in the lower left corner and the package is viewed from the top of the package as shown in Figure 1. The same reference temperature used in 5.3.2 must be used.

#### **5.4 Test method summary**

The test method using the same procedures and methods specified in JESD51-8 except that heat sources must be powered and the results obtained for a matrix of powers as described in 5.2.

The temperature rise information is reported in a table for each of the power dissipations tested as described in 4.5.

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### **6 Data reporting**

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The reporting requirements specified in the environmental specifications JESD51-2, JESD51-6, and JESD51-8 must be met in addition to reporting the temperature rise information as illustrated in Table 1.







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**STANDARD IMPROVEMENT FORM****JEDEC JESD51-31**

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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